Design and Measurement of an Inductance-Oscillator for Analyzing Inductance Impact on On-Chip Interconnect Delay

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***Abstract*— *A newly devised inductance-oscillator (iOSC) has been developed which evaluates inductance impact on on-chip interconnect delay. iOSC is a ring oscillator which is comprised of a set of wires each with different loop inductance and accurate on-chip counter. The equivalent distance to the nearest ground grid, which serves as the current return path, is varied to control wire inductance.*

A test chip using 0.13-μm node process is fabricated to demonstrate the concept of the iOSC. Four interconnect structures are implemented as imperfect coplanar waveguide, imitating clock lines or high-frequency inter-module signal lines. The structure with largest inductance variation measured 99 ps while a twisted ground structure which has small inductance variation measured 6 ps both for 3-mm wires. The experiments confirm that the inductance impact on delay has to be adequately analyzed and controlled to estimate a timing budget in high-speed LSI designs.

1. Introduction

As several hundred MHz to over GHz clock frequency is becoming commonplace, it becomes increasingly crucial to accurately predict the effects of parasitic elements on on-chip electrical waveforms. Specifically, lower metal-resistance and faster signal transition makes inductive impedance and resistance comparable [1]. The inductance impact which used to be only an off-chip issue is now also an on-chip concern [2]–[4]. Analyzing when and where to incorporate inductance for delay calculation is important [5] especially for systems-on-a-chip (SoC) development in which the design and verification are highly automated.

Wire inductance is dependent on the loop area that the current path forms. Thus inductances for the wires with equal physical dimensions can be different. In high-performance circuits, a grid structure for power and ground wires is a common way to distribute sufficient current all over the chip. Even when the grid structure is adopted, wire inductance still varies according to the relative position inside the grid. The use of analytical formulae for rapid estimation and evaluation of the inductance [6], [7], or quantitative evaluation of the inductance impact using statistical methodology have been proposed [8]. However, unknown factors still exist for modeling inductance, such as the contribution of silicon substrate to the current return path. Hence experimental measurements are important for characterization of the model and verification of the simulation result.

Morton [9] captured inductance effects of a bundle of 10 wires using a ring oscillator test chip. Kleveland et. al. [10] also proposed to use a ring-oscillator for characterizing the ratio between effective driver resistance and characteristic impedance of the wire. The ring includes source-end (near end) connection of the wire as part of the ring path to find abrupt change in oscillation frequency. In this paper, we propose an inductance-oscillator (iOSC) to quantitatively evaluate inductance impact on delay at the destination-end (far end) of the wire. Here, the iOSC is an oscillator whose oscillation frequency is determined by the different wire inductance. Specifically, we concentrate on the delay difference of the wires due to their relative position in between the power supply and ground grid lines.

This paper is organized as follows. In Section 2, the concept of the iOSC is presented. Then in Section 3, the layout and circuit design for the iOSC are described. In Section 4, we show experimental results using 0.13-μm node technology and we draw conclusions in Section 5.

2. Concept of inductance oscillator

Figure 1 shows the basic structure of the iOSC. It consists of the ring oscillator including long signal lines (LSIGs) as a part of the oscillator ring and on-chip frequency counter. The LSIGs all have equal parasitic capacitance and resistance but have different loop inductance. One LSIG is chosen at a time from which the inductance impact on delay can be evaluated by comparing oscillation frequencies of each LSIG. In the counter circuit, a 31-bit binary counter and shift register are implemented on the chip to accurately count the oscillation frequency. The counter values can be serially scanned out to SHIFT_OUT using a low frequency external clock signal SHIFT_CLK. The implementation of the counter eliminates impedance matched high-speed signal transmission systems outside the chip which sometimes introduces jitter in the count.

In the ring oscillator design we tried to share as many inverters as possible for the lines in which delays are compared because 1) delay change due to different inductance between LSIGs is expected to be small, and 2) process variation for each ring is not negligible compared with the delay change. Therefore, a ring oscillator is separated into two blocks and the LSIGs connect them. The iOSC is designed so that four LSIGs share most of the inverters. Among these wires, we compare oscillation frequencies. In order to vary inductance for each LSIG, the current return path is limited along the trunk power supply or ground lines (Vdd/Vss; AC ground) thus changing the distance between LSIG and ground.

Control signals LSEL[1:0] exclusively select a line among the LSIGs (line0 $\sim$ line3). For example, LSEL=0 (“00”)

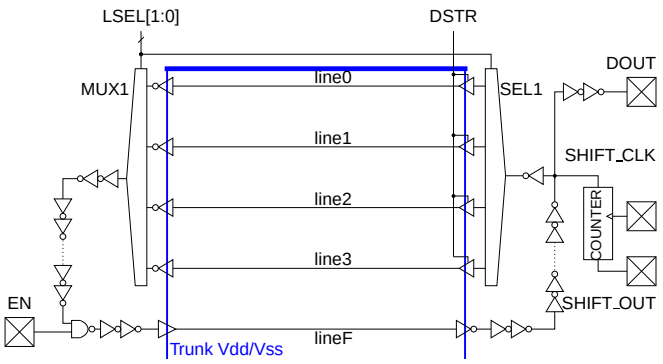

Fig. 1. Basic structure of the inductance oscillator (iOSC).

TABLE I
LOOP INDUCTANCE MATRIX FOR A STRUCTURE IN FIG. 1.

(nH/3mm)	line0	line1	line2	line3	lineF
line0	6.63	3.51	2.78	2.08	0.873
line1	3.51	6.19	3.02	2.16	0.884
line2	2.78	3.02	5.64	2.35	0.905
line3	2.08	2.16	2.35	4.84	0.965
lineF	0.873	0.884	0.905	0.965	2.83

selects line0 which is closest to the ground, and LSEL=3 ("11") selects line3 which is the farthest from ground. LineF is always used. The number of passing logic gate stages, length, and parasitic capacitances are designed to be equal. An example of the calculated loop inductance matrix for Fig. 1 is shown in Table I [11]. The width and length of the LSIGs are 5-μm and 3-mm, respectively. Ground wire width is 20-μm, and the distance between ground to line0 is 0.3-mm. The self loop inductance differs 1.4x for line0 and line3, and 2.3x for line0 and lineF.

3. Parameter design for the iOSC

3.1. Sensitivity analysis

We first conduct simple sensitivity analysis on delay change Δt due to inductance to gain insight for controlling parameters and to set parameter design targets.

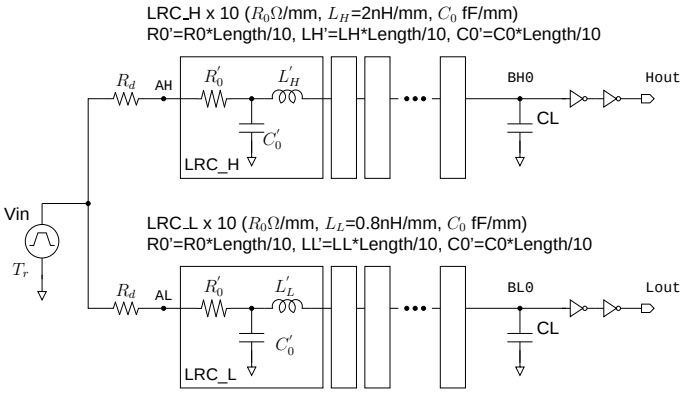

Fig. 2. A model for simulating delay change.

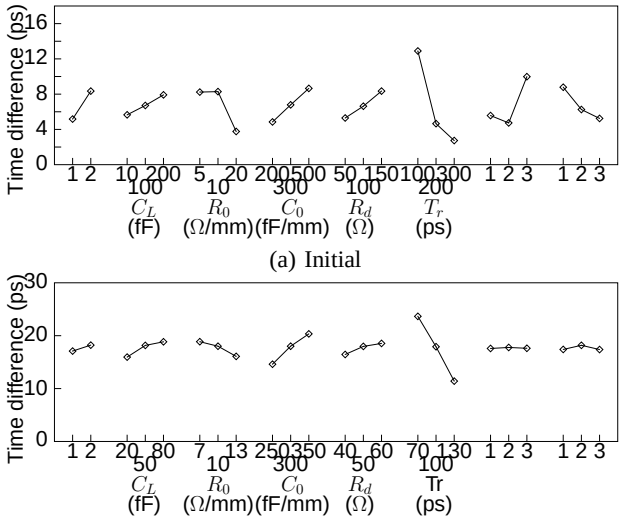

Fig. 3. Factor effect plots for delay difference $|\Delta t|$.

Figure 2 shows a simulation model to calculate delay difference due to inductance variation. The upper path has larger inductance ($L_H = 2$ nH/mm) while the lower path has smaller inductance ($L_L = 0.8$ nH/mm). Total line length is 3 mm for both paths. We evaluate $\Delta t = |t_H - t_L|$ where t_H and t_L are propagation delay from Vin to load capacitance for upper and lower path signals, respectively. We consider five parameters which are controllable in design: signal slew rate T_r, driver resistance R_d, unit length wire resistance R_0, unit length wire capacitance C_0, and receiver load capacitance C_L. The objective of this analysis is to find a robust combination of parameters for which Δt becomes sufficiently large to be able to capture as a frequency change. Using the concept of design of experiments (DoE), three levels of parameters are mapped into an L_{18} orthogonal array and then SPICE simulations are conducted.

The factor effect plot for the initial 3 control parameter levels is shown in Fig. 3(a). To design large delay difference, we set the following rules in interconnect design. Designing conversely would suppress inductance effect.

1) Signal slew T_r must be as fast as possible.
2) Wire capacitance C_0 must be large.
3) Loop resistance R_0 must be small, but it saturates at about 10 Ω/mm.
4) Larger driver resistance R_d and load capacitance C_L are better.

The sensitivity of T_r and C_0 are larger than that of the others since they make absolute current and its derivative large. Because rules 1 and 4 are generally incompatible, we give rule 1 higher priority for its larger sensitivity. The factor effect plot with the parameter targets in the center is shown in Fig. 3(b). Around the target, a robust delay difference is achieved for parameter variations.

3.2. Layout design of signal, power supply, and ground lines

Based on above analysis, we define four iOSC *structures*. Each includes different signal, power supply and ground wire configurations. Wire structures are illustrated in Fig. 4. Here a *structure* means one oscillator shown in Fig. 1 in which we can choose a wire (LSIG) from four LSIGs to compare delays.

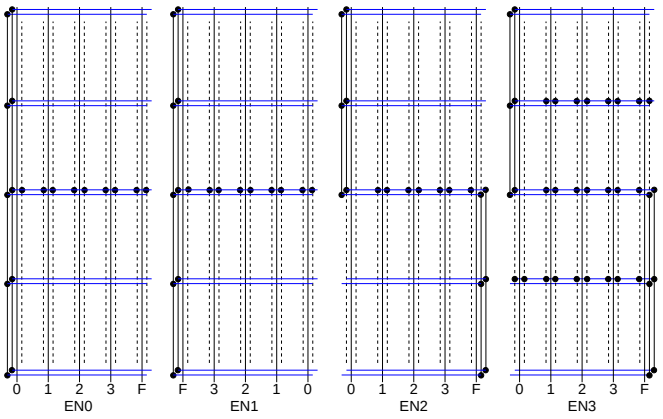

Fig. 4. Different LSIG configurations in four structures.

A structure is chosen using control signals EN[3:0]. All LSIGs use top level metal layer. The numbers 0–3 written under LSIGs represent lines0–lines3 and F represents lineF. Each LSIG employs coplanar waveguide configuration which is widely used as a clock line or interconnections between functional modules in high-speed LSI. On the both side of the LSIG (solid line), ground wires (dashed lines) run in parallel along LSIG [7], [12]. Ground wires on both sides mainly provide for constant parasitic capacitance. In order to compare cases with perfect or imperfect neighboring ground wires, both ends of the ground wires are not connected to the trunk. Vertical connections between lines in the different layers are depicted using small dots. The objectives of the structure designs are as follows:

- EN0, 1 Ground trunk encloses the structure on three sides. No ground line is on the right hand side of LSIGs, which mimics biased interconnect group location on ground grid mesh. Current returns along ground trunk making loop inductance different for each LSIG. Vias connect LSIG and ground only at the center of the line.
- EN2, 3 Ground lanes are changed from left to right at the center of LSIGs to make equivalent distance from all LSIGs to ground equal. This *twisted ground* approach is easier to implement than twisting signals [13] for grid-ground environment. The difference between EN2 and EN3 are the number of via connections to perpendicular lines. Structure EN3 uses plenty of via connections on perpendicular ground mesh to subdivide the mesh.

Ground lines, that are not illustrated for clarity, run in perpendicular to LSIGs using one layer below the top metal for all structures. Those ground lines prevent from random dummy metal fill and provide for equal capacitance.

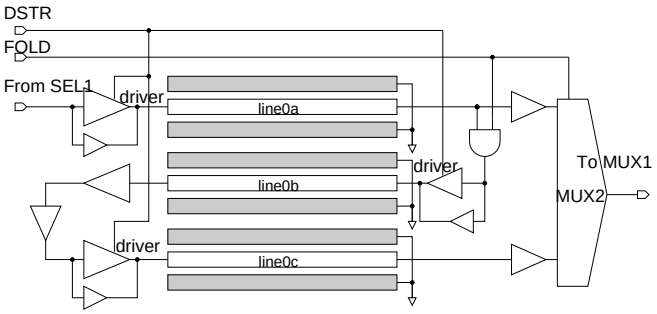

Fig. 5. Functions of DSTR and FOLD control signals.

3.3. Circuit design

Control signals EN[3:0] choose to oscillate exclusively one ring. Circuit design for the four rings is completely identical. Only layout design for LSIGs and ground differ for each ring. As shown in Fig. 1, one ring structure consists of four LSIGs (line0 – line3) and a series inverter chain including lineF which is always shared. LSEL controls the selector and multiplexer circuit. To avoid floating output, the three LSIGs that are not selected output logic "L". The wire length to selector and multiplexer are controlled to be equal. In order to make process variation impact small, 1) independent paths inside selector and multiplexer are designed to have a small number of gate stages, and 2) series inverter path stages common for all LSELs is designed to have a sufficient number of stages to achieve stable oscillation. In this chip, there are approximately 40 logic stages in shared inverters and 9 stages in independent path. The use of minimum sized transistors was avoided also to minimize process variation.

The simplified line driver circuit to describe the functions of control signals DSTR and FOLD is illustrated in Fig. 5. In order to investigate line driver strength impact on delay, driver size can be controlled by DSTR. The line driver consists of two blocks of parallel connected 3-state inverters. PMOS, NMOS transistor size W_p, W_n are 11.52, 7.2 μm respectively for DSTR=0 and 57.6, 36.0 μm for DSTR=1. Control signal FOLD folds path back and forth to enlarge inductance impact. Let us assume LSEL=0 when line0 is selected as part of the ring. If FOLD=0, then only line0a is used, but if FOLD=1 then the signal path changes to use LSIGs line0a–line0b–line0c. All lines utilize coplanar waveguide structure. Thus there are two ground lines in between neighboring signal lines, making capacitive coupling between LSIGs small enough to be ignored. The width of LSIG and coplanar ground wires are both 5 μm.

The on-chip counter consists of a 31-bit binary counter and a shift register. During oscillation, it counts occurrences of the rising edge of the oscillation waveform. After stopping the oscillation, the count results are sent to the shift register, then serially scanned out to pad SHIFT_OUT. Low frequency clock signal can be used for shift operation since it is independent of

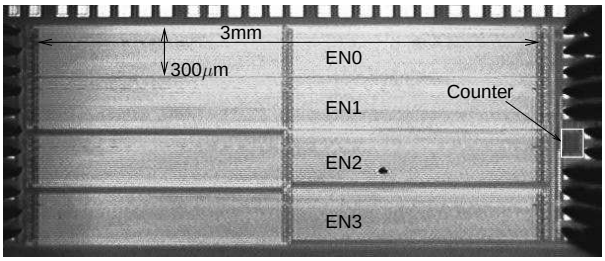

Fig. 6. Test chip micrograph.

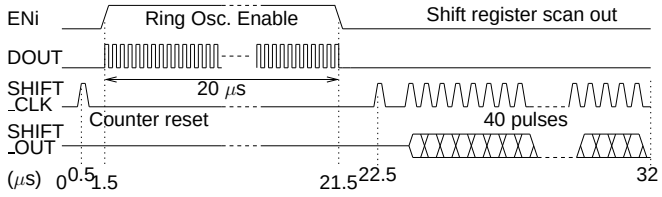

Fig. 7. Simplified timing diagram of the measurement procedure.

the ring oscillation. Dedicated power and ground are supplied for counter and other control circuits so as not to cause fluctuations in the ring oscillator power supply voltage.

4. Experimental results

We fabricated the iOSC using 0.13-μm, five metal layer process. A micro photograph of the test chip is shown in Fig. 6. Four structures selected by EN[3:0] and the location of the on-chip counter circuit is indicated. Each structure measures approximately 3-mm in length and 300-μm in width.

4.1. Oscillation frequency measurement

A simplified timing diagram of single measurement procedure is illustrated in Fig. 7. The process is summarized as follows:

1) Initialize binary counter by sending a pulse into SHIFT_CLK (at 0.5 μs).
2) Start oscillation by changing one of ENi (i=[3:0]) to "1" while keeping other ENs at "0" (1.5–21.5 μs). Bringing ENi back to "0" stops oscillation. The on-chip binary counter captures the number of rising edges of the oscillation waveform.
3) Transfer counter contents into shift register by sending a pulse into SHIFT_CLK again (22.5 μs).
4) Series pulses to SHIFT_CLK passes register contents serially to the output SHIFT_OUT in MSB to LSB order. Scanning delimiter "01 11111111" (1 fixed "0" bit and 9 (equals 40 input pulse minus 31 register length) "1" bits) closes one measurement of 32 μs.

Oscillation continues for 20 μs in this measurement. The on-chip counter accurately captures the rising edge. We used SHIFT_CLK at 10 MHz and sampling frequency of the data analyzer at 20 MHz. To verify stability of the measurement, we repeated above procedure on the same LSIGs 48 times each using a logic tester. Frequency count for the case FOLD=0 and DSTR=0, which means no wire folding and the use of weaker line driver, is shown in Fig. 8. The horizontal axis is the measurement numbers each corresponds to a measurement procedure shown in Fig. 7. Hence one point in the graph corresponds to 32 μs in time. The vertical axis is the number of oscillations. In Fig. 8, we first measure line0 (LSEL=0) in structure EN0 for 48 times in succession. Next, line1 (LSEL=1), line2 (LSEL=2), and line3 (LSEL=3) in EN0 are also measured for 48 times each. Then we move the target structure to EN1, EN2, and EN3, and the same number of measurements are repeated by selecting the appropriate lines. 48 measurements for four lines in four structures makes 768 series measurements in total.

One interesting phenomenon observed here is that for almost all cases the second measurement count increases slightly from the first one. After the peak at the second measurement, the counts gradually decrease as the measurements are reiterated. The count stabilizes after about 10 measurements or 320 μs. The maximum difference between maximum and stable count is 20 for 20 μs (about 0.43 %) in Fig. 8. The one major cause of the count change is considered due to Joule heating of the interconnect and devices. In the following, we use average count of last 32 measurements out of 48 (from 17 to 48-th measurements) as the stable counts.

The exact same measurements as Fig. 8 are repeated and compared to check long-term measurement stability. The count difference of 768 measurements was less than +2/-3, and maximum averaged count difference was +1.1/-0.5. Average error was 0.42 which is below 0.01 % compared with the total average count of 4565. This corresponds to 1.8 ps timing resolution. Thus, it was verified that the on-chip counter circuit provides enough accuracy to capture count variation due to inductance.

4.2. Structure and wire configuration dependency

Figure 9 summarizes oscillation count for DSTR=1 and FOLD=0. The horizontal axis is the structures and lines, and the vertical axis is the oscillation count for 20 μs. Since stronger drivers are used here, the count increased by about 30 percent compared with DSTR=0 case (Fig. 8) but the changes in count have the same tendency. When LSEL goes up, the count decreases for EN0 but increases for EN1. Namely, the count increases when LSEL is closer to the ground trunk because inductive impedance decreases, and vice versa. The power distribution and ground layout for line drivers are identical for the two structures but the delay changes in opposite direction by just changing the position of the ground trunk, meaning the change is not due to IR drop. Figure 10 compares count change between different DSTR and FOLD configurations. The counts are normalized using the count of line0 as a reference since each case has different oscillation frequency.

4.3. Discussion

Irrespective of the wire folding or driver strength, the oscillation counts of the lines in structures EN0 and EN3 are

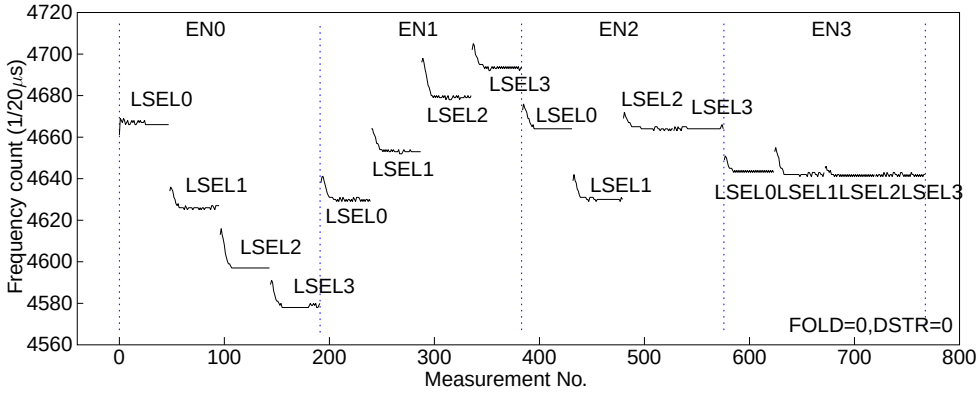

Fig. 8. Oscillation counts for 768 consecutive measurements (DSTR=0, FOLD=0) on a die.

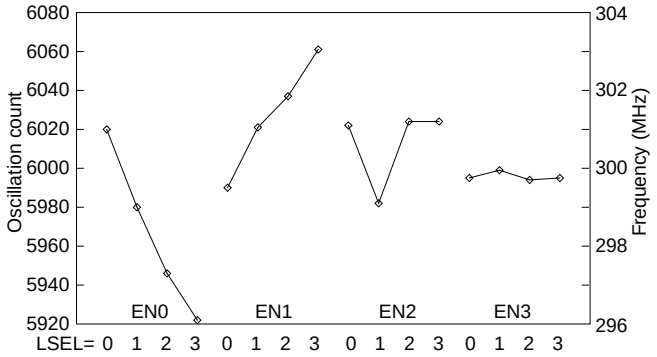

Fig. 9. Oscillation count summary for FOLD=0, DSTR=1.

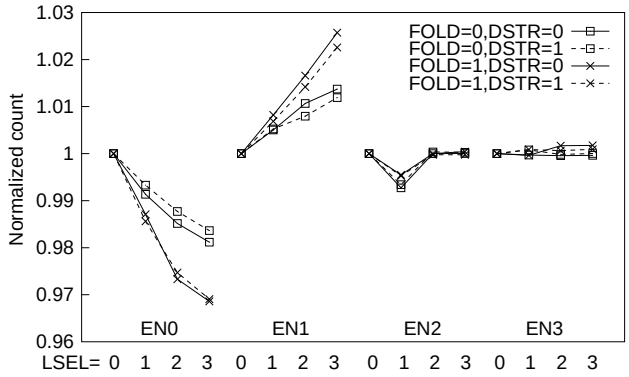

Fig. 10. Normalized oscillation count variation (count for line0 (LSEL=0) as 1).

significantly different. This result suggests that if an insufficient ground were used, unpredictable timing difference due to inductance may arise even for coplanar structures. The high-speed signals, such as clock or bus wires, that cannot allow skew between wires have to have their inductance controlled as well as their parasitic resistance and capacitance. On the other hand, the frequency counts of the lines in structures EN2 and EN3 are constant except line1 in structure EN2. Twisting ground wires equalize self-inductance and also significantly reduce mutual inductance resulting in small skew between lines.

TABLE II

MAXIMUM DELAY VARIATION ON A TYPICAL DIE.

Condition		Delay variation in ps (%)			
FOLD	DSTR	EN0	EN1	EN2	EN3
0	0	88 (1.9)	64 (1.4)	34 (0.73)	2 (0.04)
0	1	99 (1.7)	71 (1.2)	41 (0.70)	6 (0.10)
1	0	98 (3.2)	78 (2.5)	15 (0.49)	7 (0.21)
1	1	139 (3.2)	98 (2.2)	21 (0.47)	4 (0.09)

The timing difference of the LSIGs for all FOLD, DSTR conditions and structures in a typical die is summarized as Table II. The timing difference for EN0 is larger than the one in structure EN1 for all conditions. The difference between lines that gave maximum (LSEL=0; line0) and minimum (LSEL=3; line3) frequency count is 139 ps (3.2 % of averaged count) for the path folding (FOLD=1) and 99 ps (1.7 %) when the path is not folded (FOLD=0) for EN0. For EN1, difference in time between maximum (LSEL=3; line3) and minimum (LSEL=0; line0) frequency count is 98 ps (2.2 %) for the path folding (FOLD=1) case and 71 ps (1.2 %) when path is not folded (FOLD=0). One reason for EN0 having larger variation than EN1 is that in EN0, shared wire lineF is the farthest from ground trunk. It makes the average inductance of the round trip lines slightly larger than EN1.

EN2 and EN3 achieved very small variation although EN2 was deteriorated by line1 for probable layout problem. This measurement suggests that, for the high-speed interconnections, the finer ground grid must be used to provide closer return current path to achieve small skew between wires.

Table III summarizes averaged measurement results over 17 dies. The average count for the structure $\overline{n}$ is calculated as $\overline{n} = 1/17 \sum_{i=0}^{17} (\sum_{LS=0}^{4} n_{i_{LS}}/4)$ where $n_{i_{LS}}$ is the count for each LSEL in die number i. Δn is the largest absolute difference for LSELS: $\Delta n = 1/17 \sum_{i=0}^{17} (\max_{LS}(n_{i_{LS}}) - \min_{LS}(n_{i_{LS}}))$. Then averaged maximum variation $\overline{v_p}$ is expressed as $\overline{v_p} = \Delta n/\overline{n} \times 100$ (%) and σ_p is the standard deviation of v_p. Compared with EN0 and EN1, EN2 and EN3 have larger $\overline{n}$ and smaller Δn. The lines with larger inductance showed reduced average oscillation count and increased maximum count difference.

Histogram plots for averaged maximum variation $\overline{v_p}$ is

TABLE III

OSCILLATION COUNT AND ITS VARIATION FOR 17 DIES.

	Oscillation count		Count variation (%)	
EN	average $\overline{n}$	max−min Δn	average $\overline{v_p}$	deviation σ_p
0	4846.6	97.1	2.16	0.89
1	4859.7	93.0	2.06	0.76
2	4875.0	25.9	0.53	0.19
3	4887.6	24.2	0.48	0.24

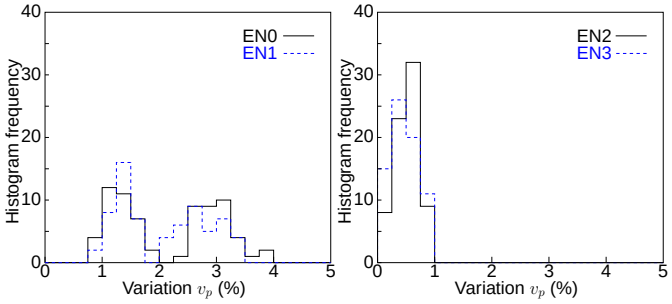

Fig. 11. Histogram plot for averaged frequency variation.

shown in Fig. 11. Figure 11 includes all combination of FOLD and DSTR. EN0 and EN1 have two peaks corresponding to the line folding. The maximum variation is about 4 % and there is no die with small variation around 0 %. On the other hand in EN2 and EN3, variation is always within 1 % and there is single (or indistinguishable) peak variation regardless of the line folding. The statistical result also confirms that EN2 and EN3, the twisted ground structures, are significantly superior to EN0 and EN1.

5. Conclusion

An inductance oscillator which selects the wires with different inductance but equal parasitic resistance and capacitance is newly devised. The impact of the on-chip inductance on delay is evaluated through test chip measurements for 3-mm coplanar lines that mimic high-speed signals such as clock lines. The following structures are measured: 1) a structure with different loop inductance by changing the distance to the ground, and 2) a structure with equal inductance by twisting the ground line to make equivalent distance the same.

A test chip using 0.13-μm node process is fabricated. An on-chip counter circuit measures the frequency count of the ring with accuracy within 0.01 % or 2 ps error. The structure with different loop inductance has a larger timing variation of 99 ps at the maximum, and the newly proposed twisted ground structure measured 6 ps variation for 3-mm wires. Statistical analysis on multi-die measurements shows that the inductance effect on delay needs to be considered when designing clock lines and module-to-module interconnections. The importance of the current return path design must be emphasized in early stages of the design.

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