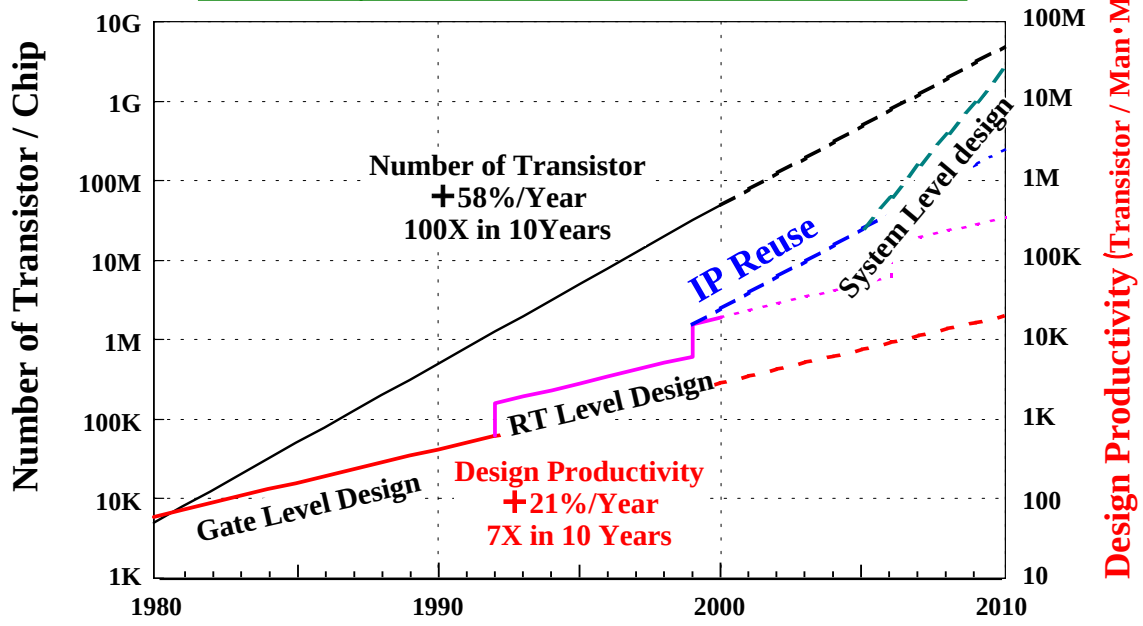
STARC Semiconductor Technology Academic Research Center

−Project ASUKA−

Call for technology innovation for efficient SoC design

Issues	1. System Level Design Automation 2. IP Reuse and IP Trading 3. Deep Sub Micron Design Technology 4. Low Power Design Technology



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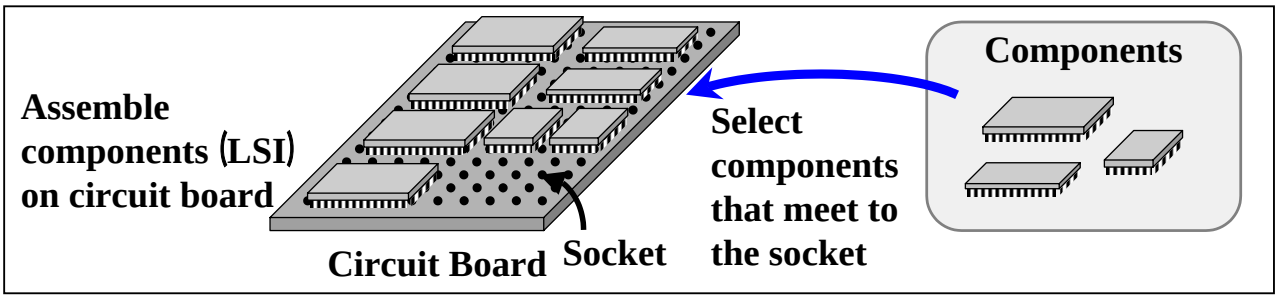

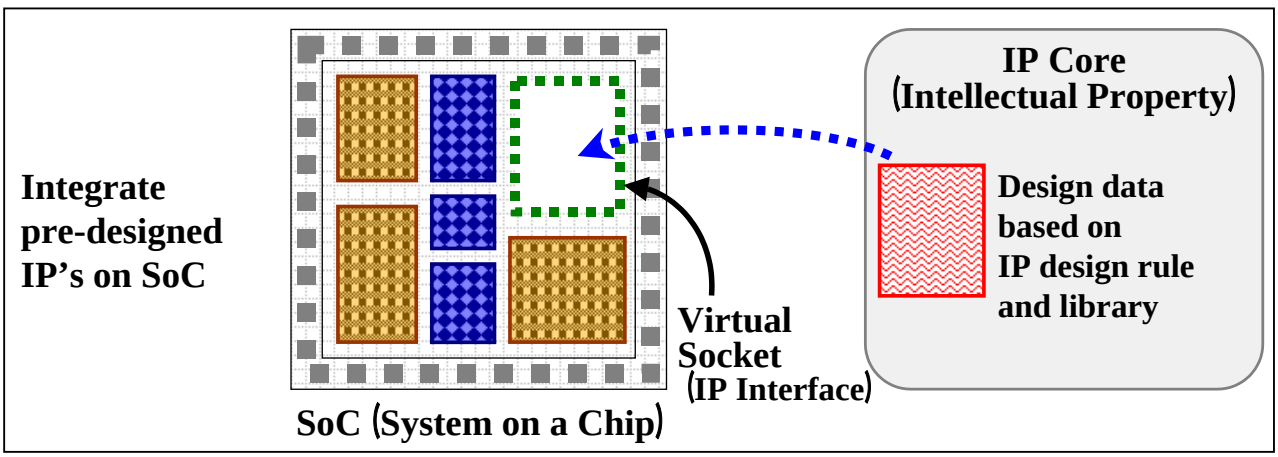

If IP design rule(geometrical design rule, library and IP interface) does not meet with SoC
→ Require IP modification → New Design/ No Reuse

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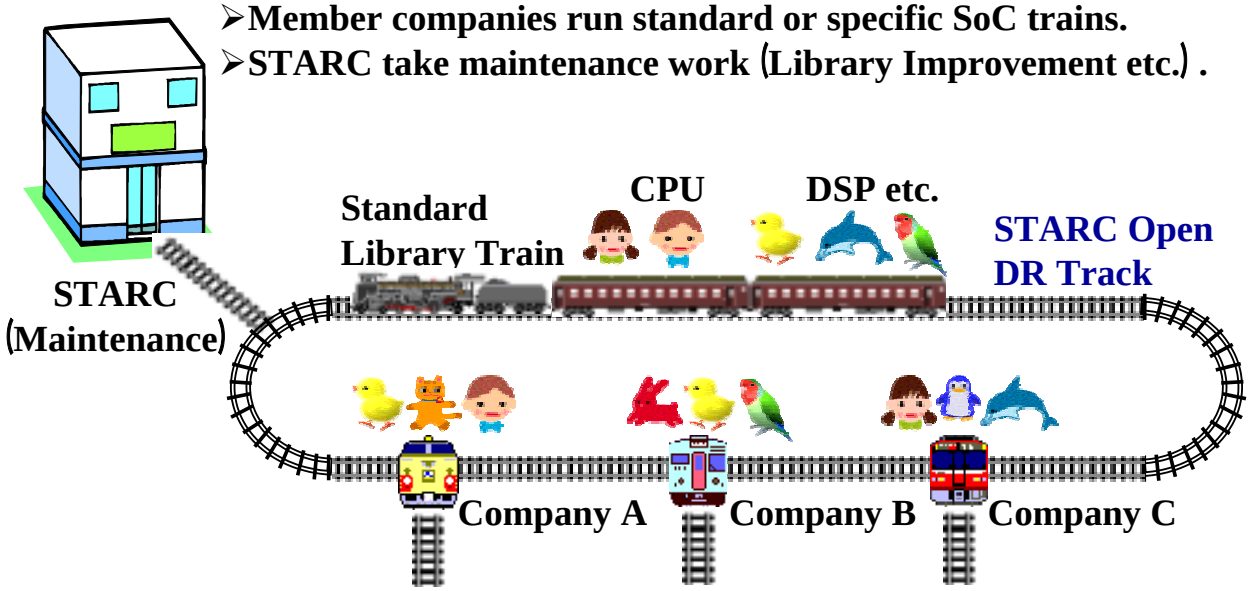
STARC Recommended Design Rule and Standard Library

- STARC runs standard library train on standard DR track.
  - Standard Library (500 Cells) Train
  - Carry IP's (CPU's, DSP's, etc. provided by member companies)
- Member companies run standard or specific SoC trains.
- STARC take maintenance work (Library Improvement etc.) .



2001.8.23

"IP-Based SoC Design Technology Set"
Technical Supplement

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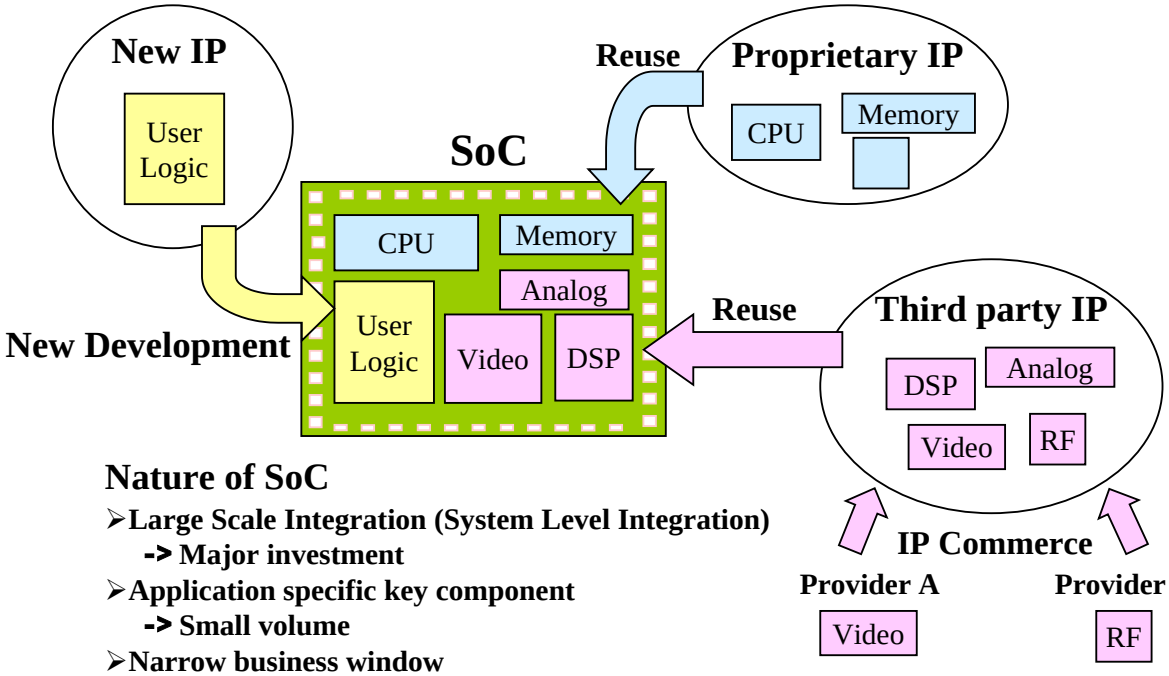
STARC
Design Technology Development Dept.
IP Reuse Group

Contents

1. Background – Issues around IP-Based SoC design technology –
2. Summary of "STARC IP-Based SoC Design Technology"
3. Si Technology for SoC -Recommended design rule and library-
4. SoC Design Infrastructure
5. Future Plan

IP Based SoC Design

−Systematic IP reuse improve design efficiency drastically−



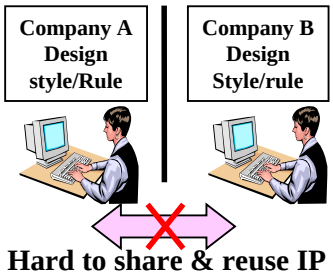
Nature of SoC

- Large Scale Integration (System Level Integration)
  -> Major investment
- Application specific key component
  -> Small volume
- Narrow business window

Issues for IP Reuse and Commerce

Current status: Many obstacles on IP reuse & commerce

- Design styles & rules are incompatible.
- Large engineering resources are necessary for re-design and re-verification.



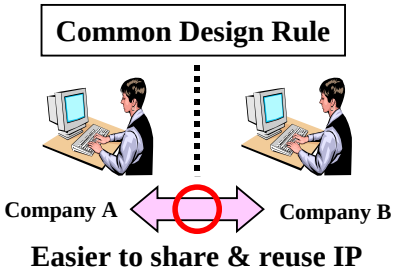
Scenario for change !

- (Scenario 1) Establish sharable Design Rule among semiconductor manufacturers and IP Vendors.
- (Scenario 2) Establish sharable set of process specifications.

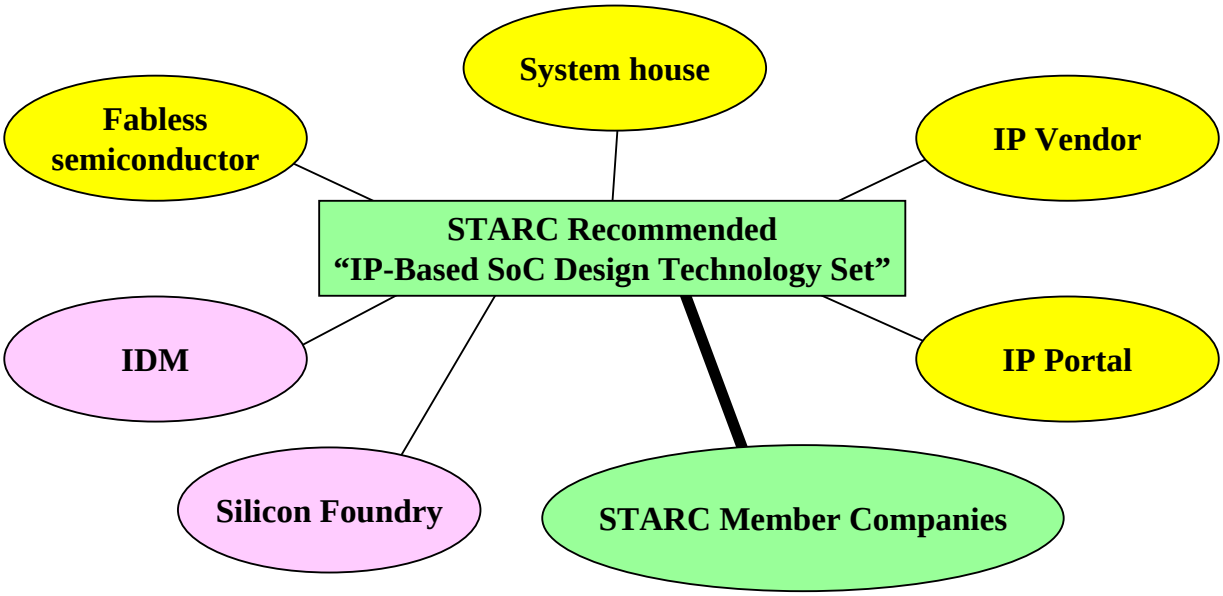
Scenario 1 has better chance compare with Scenario 2.

"STARC IP-Based SoC Design Technology Set"

- STARC has been challenging toward the scenario 1.
- Twelve STARC member companies have endorsed STARC SoC design technology set and use them in their future SoC business.
- STARC makes the technology set open to public and calls for adoption.

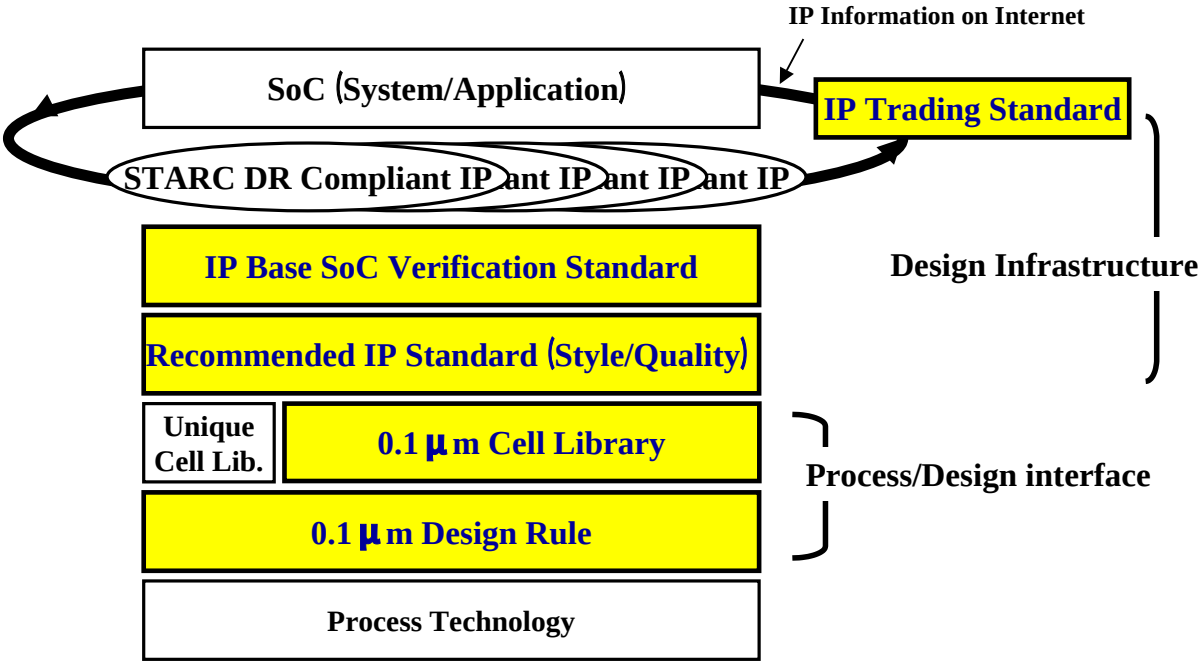


Beneficiaries of "STARC IP-Based SoC Design Technology Set"



−STARC Recommended−

"IP-Based SoC Design Technology Set"



STARC Recommended Design Rule (DR) (1)

1. Contents (Reference 1,2)

✧Geometrical Design Rule
✧SPICE Parameter set

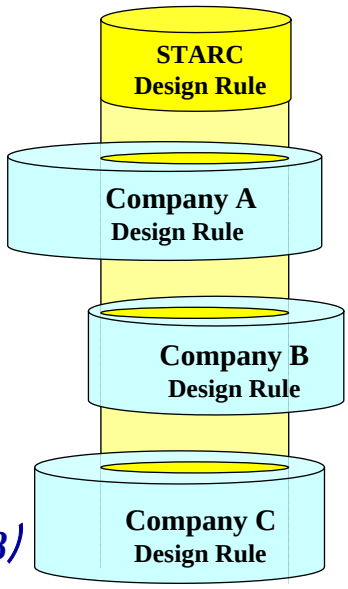
2. Expected merit

✧Adopter on DR can manufacture DR compliant IP much straightforward.
✧Compliant IP can reduce re-characterization and re-verification cost in SoC manufacturer.
✧Reduce re-engineering cost in IP Vendor.

3. Chronology

- 0.13μm STARC Recommended Design Rule (2000.9)
- *0.1 μm STARC Recommended Design Rule (2001.8)*

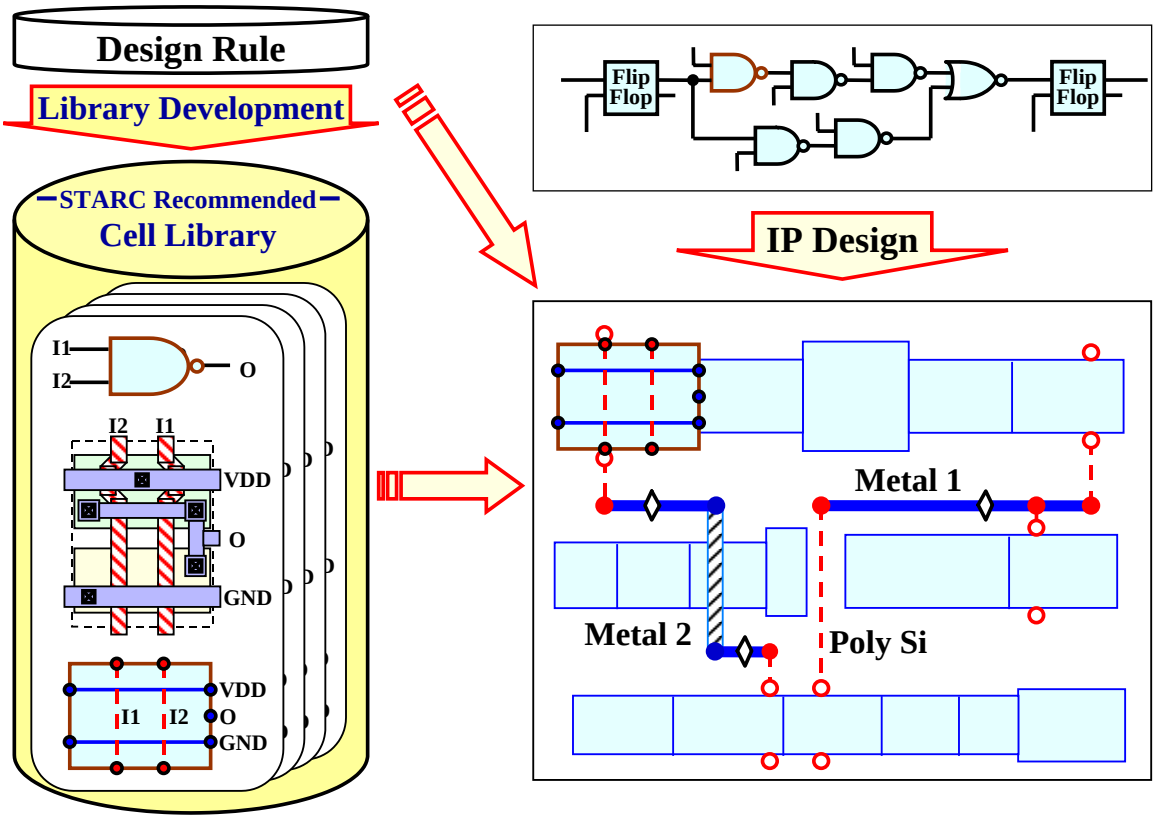
Relationship between STARC DR and individual DR



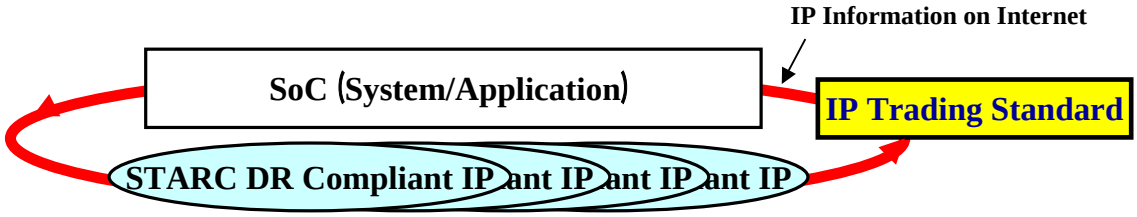
STARC Recommended Design Rule (DR) (2)

Technology Node	0.10μm	
Transistor Version	High Performance	Middle Performance
Voltage (V) :Core / I/O	1.0/2.5/3.3	1.0/2.5/3.3
Physical Gate Length (μm) :Core	0.065	0.065
Poly Pitch (μm)	0.24	0.24
Metal 1 Pitch (μm)	0.24	0.24
Metal x Pitch (μm)	0.28	0.28
Ion_n/Ion_p (μA/μm) :Core	630/275	480/200
Applications	High Speed	Core Logic

Cell Library and Cell-base IP Design



SoC Design Infrastructure (1)
−IP Trading Standard−



Easy to use/ Secure/ Inexpensive/ Reliable IP information access system is indispensable need of SoC designer.

Requirements:

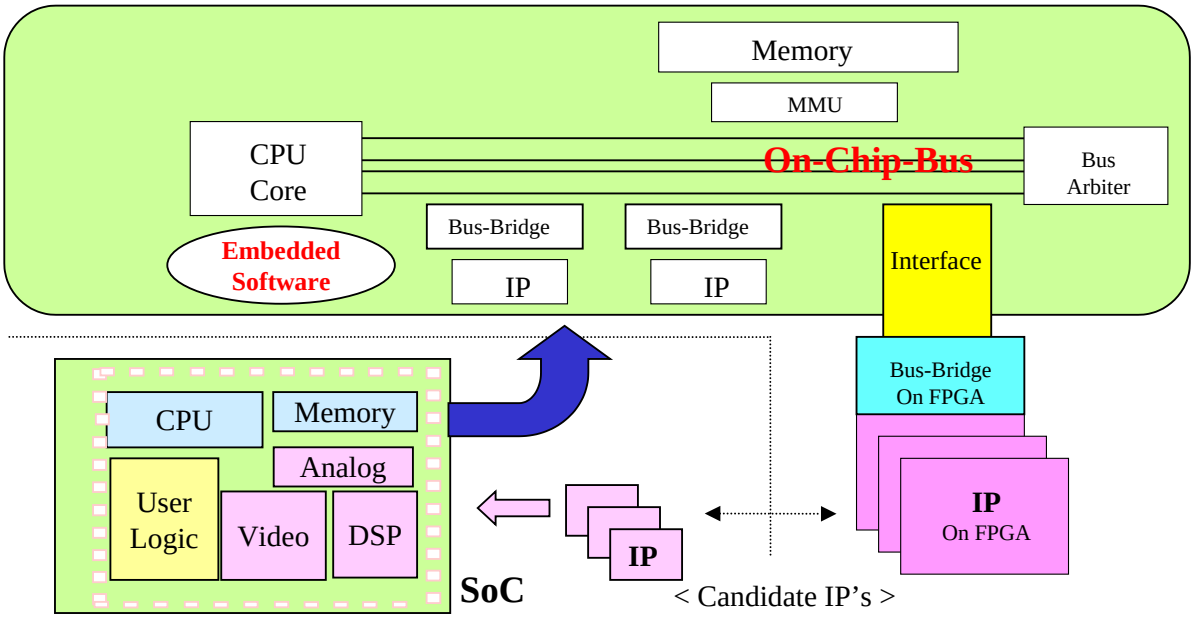
1. Access pass to outside IP information (Through Internet)
2. Integration with internal IP information system (Company dependent Intranet)
3. Guideline and mechanism for technology contamination prevention

Established IT standard for IP trading
(Standard Trade Procedure for STARC DR Compliant IP)

SoC Design Infrastructure (2)
−IP-base SoC Verification Standard−

IP-base SoC Prototyping Platform

-- Platform for Verification and IP Selection including Embedded Software --



SoC Design Infrastructure (3)
−Recommended Standards (Style Guide, Quality Standard) −

1. Establish technology standards for collaboration and communication between system and semiconductor designers (Syntactical standard)
   - Extend RTL design style guide (2000.7)
   - RTL sign off standard
   - Naming rule standard (Chip Level, Cell Level)
2. Technology standards for collaboration and communication between IP developers and IP users (Semantic standard)
3. Quality standard for IP qualification
   (IP qualification standard (Quality measure standard))

Future Plan

SoC Design Rule and Cell Library

1. 0.1um STARC Open Design Rule：Draft proposal 2001. 2Q
2. 0.1um STARC Standard Cell Library (Std.)： 2002. 4Q

(After "Std." was completed, "HS" and "LP" version will be developed.)

SoC Design Infrastructure

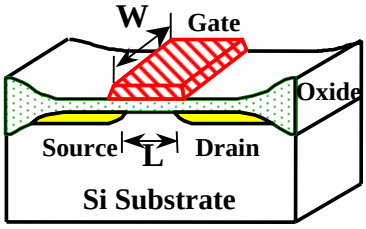
1. IP Information Delivery Standard： 2002. 1Q
2. IP Verification Standard： 2002. 2Q
3. IP Coding Standard (Syntax)： 2002. 1Q
4. IP Coding Standard (Semantics)： 2002. 1Q
5. IP Qualification Standard： 2002. 1Q

IP Trading

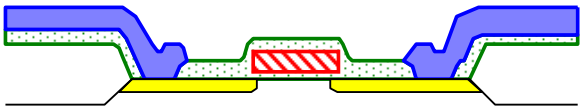
1. Develop Key IP's such as CPU, then Promote trading

(Reference 1)

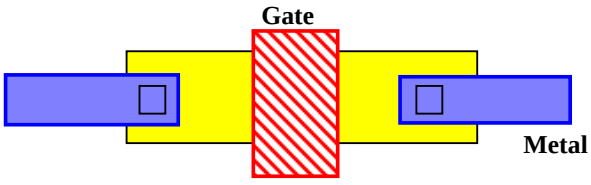
Geometrical design rule and SPICE Parameters



MOS FET (Sectional View)



(a) Cross Section
(Depend on Each Process)



(b) Top View
(Geometrical Design Rule)

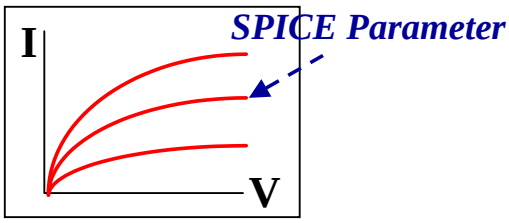
STARC Recommended Design Rule

Standardize (b) and (c)

Since geometrical design rule define physical parameters and SPICE parameter define Transistor characteristic,
IP fabricated at different Fab under same DR should have very similar performance.

Process Standardization

Standardize (a) , (b) and (c)

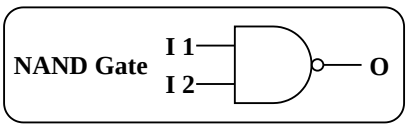


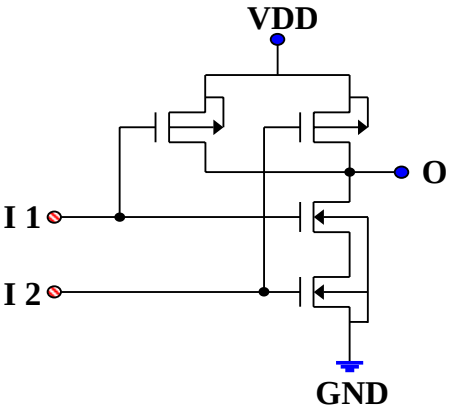
(c) Transistor Characteristic

(Reference 2)

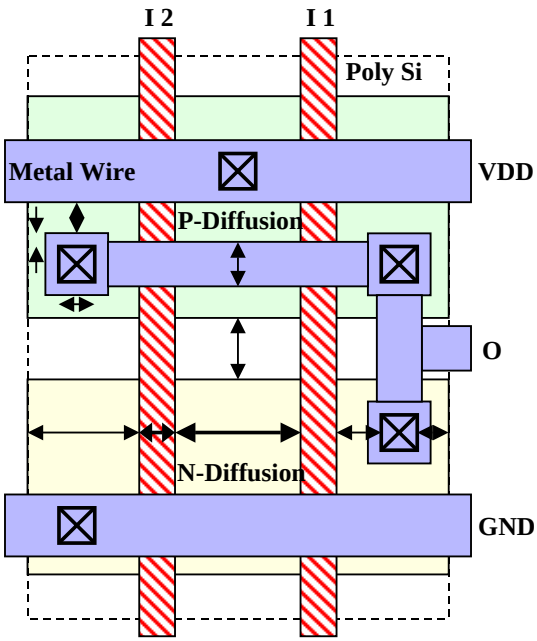
Geometrical Design Rule

Rules to design photo mask, including minimum width/ space/ overlap etc.





(1) Transistor Circuit

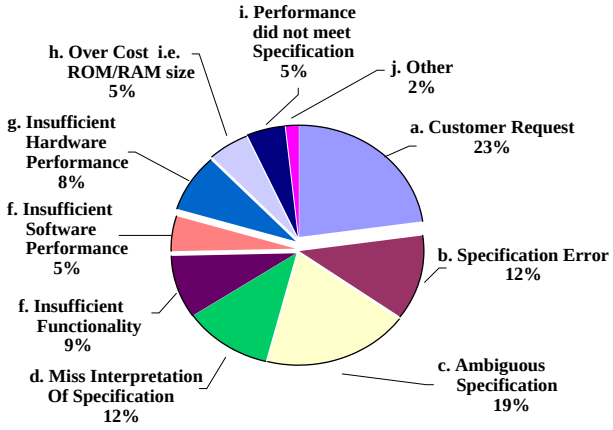


(2) Cell Layout

(Reference 3)

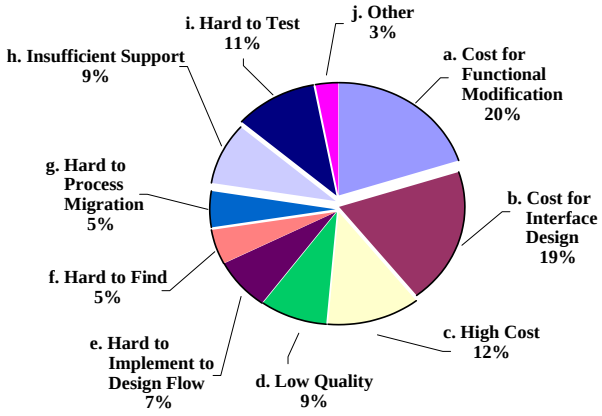
Problem on System Level Design

Liquid System Specification



- Specification Error, Ambiguity, Miss Interpretation → 43%
- Unable to Meet the specification → 32%

Obstacles on IP Reuse



- Require Customize Work → 44%
- Hard to Test → 11%
- Hard to Implement to Design Flow → 7%

Source: FY2000 SLD WG report：Proposal for System Level Design and System Level Design Language

Issues **Lack of technology standard for SoC/IP Design**