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## Cadence Software Validated on STARC QA Database to Help STARC Members Ensure Advanced Chip Design Quality

### *Validation Suite Ensures High Software Quality for Chip Design*

SAN JOSE, Calif., Jan. 28, 2010-- Cadence Design Systems, Inc. (NASDAQ: CDNS), the leader in global electronic design innovation, and Semiconductor Technology and Academic Research Center (STARC), the Japan semiconductor industry consortium, today revealed an ongoing collaboration to leverage STARC's regression suites to ensure the high quality of electronic design automation (EDA) software for advanced chip design. The regression suites and validation flow were developed by STARC and its member companies to qualify EDA software for use by consortium members.

Already facing tremendous pressure to create new, extremely complex semiconductor designs under tight deadline, today's design engineers demand the highest possible level of confidence in their design software. As part of its mission to assist member companies in evaluating and building their design flows, STARC has developed the validation methodology to test new design software before its members embark on advanced projects.

"One of our most important missions is to help our members ensure the quality and accuracy of their chip design software," said Nobuyuki Nishiguchi, vice president and general manager, Development Department 1 at STARC. "This methodology allows us to accomplish our mission using tests developed by STARC and the members themselves, thereby ensuring the maximum fit with their requirements."

Using common test suites developed and consolidated by STARC, the methodology includes regression tests for large designs to quickly identify differences between new versions of tools. Test results are stored in STARC's quality assurance

database (QA database) and reports are sent to STARC member companies. This process helps designers to quickly build quality flows that are appropriate to their needs. The system currently covers Cadence® Conformal® Constraint Designer and Encounter® Timing System., [Encounter Digital Implementation System's](#) Statistical Static Timing Analysis (SSTA), and Encounter RTL Compiler.

“Mission critical software quality continues to be our number one priority. We're pleased to work with STARC on the software validation flow with real customer designs,” said Dr. Chi-Ping Hsu, senior vice president of research and development in the Implementation Group at Cadence. “This collaboration uniquely positions Cadence as the industry leader in quality focus, and ensures that validation and test results are meeting designers' requirements.”

### **About Cadence**

Cadence enables global electronic design innovation and plays an essential role in the creation of today's integrated circuits and electronics. Customers use Cadence software and hardware, methodologies, and services to design and verify advanced semiconductors, consumer electronics, networking and telecommunications equipment, and computer systems. The company is headquartered in San Jose, Calif., with sales offices, design centers, and research facilities around the world to serve the global electronics industry. More information about the company, its products, and services is available at [www.cadence.com](http://www.cadence.com).

### **About STARC**

The Semiconductor Technology Academic Research Center, STARC, is a research consortium co-founded by major Japanese semiconductor companies in December 1995. STARC's mission is to contribute the growth of the Japanese semiconductor industry by developing leading-edge SoC design technologies.

For more information, please visit <http://www.starc.jp/index-e.html>

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