STARC

# News Release

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Semiconductor Technology Academic Research Center

## STARC releases Updated Version of the “TL Modeling Guide” for Transaction Level Design

The Semiconductor Technology Academic Research Center (STARC, President & CEO Katsuhiro Shimohigashi) has developed a new modeling guide which describes standard practices for Transaction Level Modeling (TLM) used in the design of electronic systems. The "TL Modeling Guide second edition" supports a design methodology which is independent of specific EDA tools and smoothes the interface between system design and LSI design. This new, updated edition is compliant with OSCI (Open SystemC Initiative) TLM2.0 SystemC standards and enables highly reusable and interoperable models to be created.

The demand on designers of electronic devices to develop increasingly complex, large scale LSI has revealed design issues that cannot be resolved using conventional RTL based methodologies. Transaction level design was introduced to raise the level of abstraction and solve these issues by enabling critical areas such as the exploration of architectural design and software/hardware co-design to be implemented at the early stages of a design.

In order to establish a seamless, integrated "standard design methodology" from system design through to real chip implementation, STARC investigates semiconductor industry "best practices" and then develops and promotes design methodology standards and recommendations (*1). The "TL Modeling Guide first edition" was defined in January 2008 as a part of these activities with the purpose of establishing a standard system design methodology using TLM. The original guide was based upon the OSCI TLM1.0 and the “TL Modeling Guide second edition” has been developed to incorporate the new features included in TLM2.0.

As a TLM reference, the guide defines standards in three areas (abstraction level, model structure, and, communication API) and then illustrates how the standards can be put into practice by designing the models for an example device. Because the new edition is based on TLM2.0 features such as coding styles, sockets, the generic payload, and the base protocol, it is possible to develop models which offer high reusability and interoperability.

By releasing the TLM reference, STARC hopes to promote the widespread of the TLM models which are less dependent on a specific LSI vendor or an EDA tool, and enable sharing of design information between electronic systems developers and SoC designers. It will be hoped to expand the use of TLM in the design community.

The guide has been developed with semiconductor industry best practices by experts from STARC's clients companies for more than half a year. STARC plans to offer the modeling guide widely and openly. It will be updated through the active support and participation of those interested in system design technologies.

Kenichi Kanehara of Toshiba Corporation, who is a chairman of the Design Standard Support Committee of STARC, said "I expect that the TL Modeling guide second edition will accelerate the wide use of TL Modeling for the system level design in the industry thanks to the quick incorporation of OSCI TLM2.0 into the guide. "

The "TL Modeling Guide second edition" will be introduced at EDSFair 2009 (January 22-23, 2009, Pacifico Yokohama, Japan) at both the STARC booth and in Exhibitor Seminars.

Electronic versions (PDF file) can be downloaded from the STARC homepage.

A printed version is also available for purchase (in Japanese only).

http://www.starc.jp/tlmg/index-j.html (Japanese)

http://www.starc.jp/tlmg/index-e.html (English)

***1: Technical standards, guidebooks, etc. which STARC has released.**

1) RTL Design Style Guide (Japanese version only)
   http://www.starc.jp/bookstore/index-j.html
2) IP Functional Verification Guide (Japanese version only)
   http://www.starc.jp/ipfvg/index-j.html
3) STIL Usage Guide
   http://www.starc.jp/stil/top-e.html

**About STARC**

Semiconductor Technology Academic Research Center (STARC) was established in December 1995 with investment from Japan's leading semiconductor suppliers to reinforce semiconductor design capability. Since its inception, STARC has been conducting joint research with universities and the semiconductor industry to strengthen the bases of research in the field of semiconductor technology at domestic universities.

The outcomes of these activities have now been utilized industry-wide in Japan through the transfer of technologies to investing companies to help their businesses, the documenting of technical standards and the licensing of technologies to partner companies for commercialization. For more information about STARC and its research, visit http://www.starc.jp/index-e.html.

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