News Release

January 18th 2008

Semiconductor Technology Academic Research Center

STARC releases TL Modeling Guide as reference manual for Transaction Level Design

The Semiconductor Technology Academic Research Center (STARC, President & CEO Katsuhiro Shimohigashi) today announced the release of the "TL Modeling Guide." The guidelines which STARC has developed describe standard practices for Transaction Level Modeling (TLM) used in the design of electronic systems. The guide supports a design methodology which is independent of specific EDA tools and is intended to smooth the interface between system design and LSI design.

The demand on designers of electronic devices to develop increasingly complex, large scale LSI has revealed design issues that cannot be resolve using conventional RTL based methodologies. Transaction level design was introduced to raise the level of abstraction and solve these issues by enabling critical areas such as the verification of architectural design and software/hardware co-verification to be implemented in the early stages of a design.

In order to establish a seamless, integrated "standard design methodology" from system design through to real chip implementation, STARC investigates semiconductor industry "best practices" and then develops and promotes design methodology standards and recommendations (*1). The "TL Modeling Guide" was defined as a part of these activities with the purpose of establishing a standard system design methodology using TLM.

As a TLM reference, the guide defines standards in three areas (abstraction level, model structure, and, communication API) and then illustrates how the standards can be put into practice by designing the models for an example device

By releasing the TLM reference and reducing the dependence on a specific company or a tool STARC hopes to promote the distribution of LSI vendor and EDA tool free TLM, enable sharing of design information between electronic systems developers and SoC designers and thus expand the use of TLM in the design community.

The guide has condensed semiconductor industry best practices through an intensive review process conducted by experts from STARC's 11 clients companies over a period of more than half a year. STARC plans to offer the modeling guide widely and openly. It will be updated through the active support and participation of those interested in system design technologies.

“This guide summarizes the newest technology and know-how in TL design from NEC Electronics, OKI, Renesas Technology, Sony, and Toshiba," said Seiichi Nishio of Toshiba Corporation's and chairman of the System Level Design Support Committee which has been involved in the development of the guide. "I expect that adoption of TL Modeling for actual product design will now spread rapidly thanks to the modeling standardization described in this guide.”

"Mentor Graphics performed evaluations of the actual STARC models," said Simon Bloch, general manager, Design Creation and Synthesis Division, Mentor Graphics Corporation. "Our

support of STARC's communication API will enable smooth interoperabilty between Mentor tools and STARC models at the eleven STARC consortium companies."

Kenichi Kanehara of Toshiba Corporation, who is chairman of the Design Standard Support Committee said "The guide is aimed at not only the semiconductor industry but also at system designers in the wider electronic systems industry. As a result it is expected that use of the TL modeling guide will expand cooperation between system designers and LSI designers further. "

The "TL Modeling Guide" will be introduced at EDSFair 2008 (January 24-25, 2008, Pacifico Yokohama, Japan) at both the STARC booth and in exhibition seminars.

An electronic versions (PDF file) can be downloaded from the STARC homepage.

A printed version is also available for purchase (Japanese only).

http://www.starc.jp/tlmg/index-j.html (Japanese)

http://www.starc.jp/tlmg/index-e.html (English)

***1: Technical standards, guidebooks, etc. which STARC has released.**

1) RTL Design Style Guide（Japanese only）
2) STIL Usage Guide

About Mentor Graphics

Mentor Graphics Corporation (NASDAQ: MENT) is a world leader in electronic hardware and software design solutions, providing products, consulting services and award-winning support for the world's most successful electronics and semiconductor companies. Established in 1981, the company reported revenues over the last 12 months of over $825 million and employs approximately 4,300 people worldwide. Corporate headquarters are located at 8005 S.W. Boeckman Road, Wilsonville, Oregon 97070-7777. World Wide Web site: http://www.mentor.com/.

About STARC

Semiconductor Technology Academic Research Center (STARC) was established in December 1995 with investment from Japan's leading semiconductor suppliers to reinforce semiconductor design capability. Since its inception, STARC has been conducting joint research with universities and the semiconductor industry to strengthen the bases of research in the field of semiconductor technology at domestic universities.

The outcomes of these activities have now been utilized industry-wide in Japan through the transfer of technologies to investing companies to help their businesses, the documenting of technical standards and the licensing of technologies to partner companies for commercialization. STARC is co-funded by 11 member companies including Fujitsu Limited, Matsushita Electric Industrial Co., Ltd., NEC Electronics Corporation, Oki Electric Industry Co.,Ltd., Renesas Technology Corporation, Rohm Co., Ltd., Sanyo Semiconductor Co., Ltd., Seiko Epson Corporation, Sharp Corporation, Sony Corporation, and Toshiba Corporation. For more information about STARC and its research, visit http://www.starc.jp/index-e.html.

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